

REMARKS/ARGUMENT

By this amendment Applicants amend the Abstract to be: "A method and apparatus for transferring a data block between a flash memory and a memory controller and computing an error correction code while transferring said data block." The Abstract is now technically correct and fairly describes the claimed invention. It does not refer to purported merits or speculative application of the invention and does not compare the invention to the prior art.

1) Claims 1-4, 6-10, 12-16 and 18-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston (US 6,906,961) in view of Kikuchi (US 6,131,139). Applicants respectfully traverse this rejection, as set forth below.

Claim 1 requires and positively recites a method, comprising the steps of: "transferring a data block between a flash memory and a memory controller" and **"computing an ECC for said data block while transferring the data block"**.

Claim 6 requires and positively recites, a system, comprising: "a flash memory", "a controller coupled to the flash memory" and "wherein said controller shifts a data block between the flash memory and the controller **while computing an ECC for said data block**".

Claim 12 requires and positively recites, a system comprising: "a means for storing a data block", "a means for controlling the data block", "a **means for computing an ECC of the data block**" and "a means for shifting the data block between the means for storing and the means for controlling **while computing an ECC for said data block**".

Claim 18 requires and positively recites a memory controller adapted to couple to a memory, comprising: “a memory interface” and **“an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory”**.

In contrast, Eggleston discloses a flash memory device, system, and data handling routine that implement a distributed erase block sector user/overhead data scheme that splits the user data and overhead data and stores them in differing associated erase blocks (Abstract, lines 1-4). Examiner admits that Eggleston does not disclose “a controller shifts a data block between the flash memory and the controller while computing an ECC for said data block”, as applied to claim 6 (Office Action, page 3, lines 4-6); “means for simultaneously computing an ECC of the data block” and “means for shifting the data block between the means for storing and means for controlling while computing an ECC for said data block” (Office Action, page 4, lines 1-4). Examiner’s admission, however, applies also to “an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory”, as required by Claim 18.

Examiner relies upon Kikuchi as teaching the above-highlighted omissions in Eggleston. Applicants respectfully point out that while Kikuchi discloses shifting data between a flash memory and a controller, and even mentions error correcting and checking, it does NOT teach or suggest **“computing an ECC for said data block while transferring the data block”**, as required by Claim 1; or **“wherein said controller shifts a data block between the flash memory and the controller while computing an ECC for said data block”**, as required by Claim 6; or **“a means for computing an ECC of the data block”** and **“a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block”**, as required by Claim 12; or **“an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory”**, as required by Claim 18. Applicants request that Examiner specifically identify the location of the above high-lighted elements in Kikuchi, or withdraw the rejection.

In proceedings before the Patent and Trademark Office, “the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art”. *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). “The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**”, *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lahu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious “modification” of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or “template” to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, “all words in a claim must be considered in judging the patentability of that claim against the prior art.” *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable

expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claims 1, 6, 12 and 18 are patentable under 35 U.S.C. § 103(a).

I. Motivation to Combine

Examiner states that it would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Eggleston with the flash memory device as disclosed by Kikuchi for the reasons that, “doing so would provide a memory reading control apparatus capable of reading data stored in the same memory addresses of a plurality of semiconductor memories and thus improving the performance of the memory system” (Office Action, page 3, lines 11-15). Applicants respectfully disagree that the above motivation to combine has anything to do with the claim elements at hand. Neither Eggleston nor Kikuchi, alone or in combination, teach or suggest, “computing an error correction code (ECC) WHILE transferring a block of data between a flash memory and a memory controller”. As such, any combination of Eggleston and Kikuchi fails to teach or suggest, “computing an ECC for said data block **while transferring the data block**”, as required by Claim 1; “wherein said controller shifts a data block between the flash memory and the controller **while computing an ECC for said data block**”, as required by Claim 6; “a **means for computing an ECC** of the data block” AND “a means for shifting the data block between the means for storing and the means for controlling **while computing an ECC for said data block**”, as required by Claim 12; and “**an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory**”, as required by Claim 18. According, all of the elements of Claims 1, 6, 12 and 18 are not taught or suggested by any combination of the Eggleston and Kikuchi references.

Moreover, one of ordinary skill in the art at the time of the present invention would not think to combine the disclosure of Eggleston with Kikuchi to arrive at the present invention. Moreover, Examiner has failed to find any teaching or suggestion in either reference that would suggest such a combination. Even a statement that modifications of the prior art to meet the claimed invention would have been “well within the ordinary skill of the art at the time the claimed invention was made” because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). See also *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000) (Court reversed obviousness rejection involving technologically simple concept because there was no finding as to the principle or specific understanding within the knowledge of a skilled artisan that would have motivated the skilled artisan to make the claimed invention); *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999) (The level of skill in the art cannot be relied upon to provide the suggestion to combine references.).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. “The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art.” *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Here, there is no teaching or suggestion to combine Eggleston with Kikuchi apart

from Examiner's improper hindsight in view of the instant specification. Thus, claims 1, 6, 12 and 18 are patentable under 35 U.S.C. § 103(a).

II. Reasonable Expectation of Success

Moreover, there is no indication that Examiner's proposed combination of Eggleston and Kikuchi would result in an apparatus that would enable "computing an error correction code (ECC) WHILE transferring a block of data between a flash memory and a memory controller". Thus, Examiner's proposed modification would offer no reasonable expectation of success to one of ordinary skill in the art at the time of the invention in order to arrive at the claimed invention.

III. All Claim Limitations

Finally, Examiner's proposed combination of Eggleston with Kikuchi fails to teach or suggest all the claim limitations. Neither Eggleston nor Kikuchi, alone or in combination, teach or suggest, "computing an error correction code (ECC) WHILE transferring a block of data between a flash memory and a memory controller". As such, any combination of Eggleston and Kikuchi fails to teach or suggest, **"computing an ECC for said data block while transferring the data block"**, as required by Claim 1; "wherein said controller shifts a data block between the flash memory and the controller **while computing an ECC for said data block**", as required by Claim 6; **"a means for computing an ECC of the data block"** and **"a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block"**, as required by Claim 12; and **"an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory"**, as required by Claim 18. For all the foregoing reasons, Claims 1, 6, 12 and 18 are patentable under 35 U.S.C. § 103(a) over Eggleston in view of Kikuchi.

Claims 2-4, 7-10, 13-16 and 19-23 stand allowable as depending directly, or indirectly, from allowable claims and by including further limitations not taught or suggested by the references of record.

Claim 2 further defines the method of claim 1, wherein transferring the data block comprises transferring the data block between a NAND Flash memory and the memory controller. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 3 further defines the method of claim 1, further comprising: "storing a first portion of the ECC in a first register" and "storing a second portion of the ECC in a second register if the first register is full". Claim 3 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 4 further defines the method of claim 3, wherein storing in a second register comprises selecting the second register using a switching mechanism. Claim 4 depends from Claim 3 and stands allowable for the same reasons set forth above in support of the allowance of Claim 3.

Claim 7 further defines the system of claim 6, wherein the flash memory is a NAND Flash memory. Claim 7 depends from Claim 6 and stands allowable for the same reasons set forth above in support of the allowance of Claim 6.

Claim 8 further defines the system of claim 6, further comprising: "storing a first portion of the ECC in a first register" and "storing a second portion of the ECC in an alternate register if the first register is full". Claim 8 depends from Claim 6 and stands allowable for the same reasons set forth above in support of the allowance of Claim 6. Moreover, there is no teaching in Eggleston or Kikuchi that a first portion of the ECC goes

to a first register and another portion of the ECC goes to an alternate register if the first register is full.

Claim 9 further defines the system of claim 8, wherein the controller transfers contents of all registers to memory if all registers are full. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, there is no teaching in Eggleston or Kikuchi that the controller transfers contents of ALL registers to memory if all registers are full.

Claim 10 further defines the system of claim 8, further comprising a switch to select the alternate register. Claim 10 depends from Claim 8 and stands allowable for the same reasons set forth above in support of the allowance of Claim 8. Moreover, there is no teaching in Eggleston or Kikuchi that a switch is used to select the alternate register.

Claim 13 further defines the system of claim 12, wherein the means for storing is a NAND Flash memory. Claim 13 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowance of Claim 12.

Claim 14 further defines the system of claim 12, further comprising: “storing the ECC in a first register” and “storing the ECC in an alternate register if the first register is full”. Claim 14 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowance of Claim 12.

Claim 15 further defines the system of claim 12, further comprising transferring contents of at least one register to memory if all registers are full. Claim 15 depends from Claim 12 and stands allowable for the same reasons set forth above in support of the allowance of Claim 12.

Claim 16 further defines the system of claim 14, further comprising a switch to select the alternate register. Claim 16 depends from Claim 14 and stands allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover, there is no teaching in Eggleston or Kikuchi that a switch is used to select the alternate register.

Claim 19 further defines the memory controller of claim 18, further comprising: “a switching mechanism coupled to the ECC engine” and “a register bank coupled to the switching mechanism, comprising at least one register; wherein the ECC engine stores the ECC in a register selected by the switching mechanism, the register having space available for ECC storage”. Claim 19 depends from Claim 18 and stands allowable for the same reasons set forth above in support of the allowance of Claim 18.

Claim 20 further defines the memory controller of claim 18, wherein transferring a data block comprises transferring the data block between the ECC engine and a flash memory. Claim 20 depends from Claim 18 and stands allowable for the same reasons set forth above in support of the allowance of Claim 18.

Claim 21 further defines the memory controller of claim 18, wherein transferring a data block comprises transferring the data block between the ECC engine and a NAND Flash memory. Claim 21 depends from Claim 18 and stands allowable for the same reasons set forth above in support of the allowance of Claim 18.

Claim 22 further defines the memory controller of claim 18, wherein the ECC engine transfers a data block by reading the data block from memory. Claim 22 depends from Claim 18 and stands allowable for the same reasons set forth above in support of the allowance of Claim 18.

Claim 23 further defines the memory controller of claim 18, wherein the ECC engine transfers a data block by writing the data block to memory. Claim 23 depends from Claim 18 and stands allowable for the same reasons set forth above in support of the allowance of Claim 18.

2) Claims 5, 11 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Eggleston (US 6,906,961) in view of Kikuchi (US 6,131,139), as applied to claim 1, 6 and 12 above, and further in view of Acton (US 6,594,792). Applicants respectfully traverse this rejection, as set forth below.

Claim 5 further defines the method of claim 1, wherein computing the ECC comprises performing the exclusive-or function.

Claim 11 further defines the system of claim 6, wherein computing the ECC comprises performing the exclusive-or function.

Claim 17 further defines the system of claim 12, wherein computing the ECC comprises performing the exclusive-or function.

Examiner admits that Eggleston and Kikuchi do not disclose a system, wherein computing the ECC comprises performing the Exclusive-OR function. However, the limitation is obvious and well known in the art. Examiner goes on to determine that it would have been obvious to a person of ordinary skill in the art, at the time of the invention to improve upon the data processing system, as disclosed by Acton. By doing so a different error correction code may be used which provides double-bit or greater error correction capability.

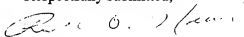
Applicants respectfully respond that Acton suffers from the same omission as that of Eggleston and Kikuchi. More particularly, Acton fails to teach or suggest, **“computing an ECC for said data block while transferring the data block”**, as required by Claim 1; “wherein said controller shifts a data block between the flash memory and the controller **while computing an ECC for said data block**”, as required by Claim 6; **“a means for computing an ECC of the data block”** and **“a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block”**, as required by Claim 12; and **“an ECC engine that computes an ECC while transferring a data block between the ECC engine and memory”**, as required by Claim 18. Any combination of Acton, Eggleston and Kikuchi suffers the same omission. As such, the 35 U.S.C. 103(a) rejection of Claims 5, 11 and 17 is improper and must be withdrawn.

Moreover, even had Acton provided such additional teaching, nowhere does Examiner support his motivation to combine with teaching from the cited references or any other prior art. Supposition not supported by fact is not sufficient evidence of motivation.

New Claims 24-26 stand allowable for depending from allowable claims.

Accordingly, Claims 1-26 stand allowable. Applicants respectfully request withdrawal of the rejections and allowance of the application as the earliest possible date.

Respectfully submitted,



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